UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,130	11/15/2000	Michael J. Bowes	108339-09058	8854

32294 7590 05/10/2004

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
MOORE JR, MICHAEL J	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,130	BOWES, MICHAEL J.	
	Examiner	Art Unit	
	Michael J. Moore, Jr.	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (U.S. 6,556,583) in view of Kosco (U.S. 5,793,236).

Regarding claim **1**, Hayashi et al. teaches a receiver circuit 9 (internet port interface controller) that contains latch circuits 901, 902, and 903 (memory) and transmission line 200 (data connection bus with high performance interface) in Figure 17. The transmission line 200 is connected to latch circuits 901, 902, and 903 (output drivers), which are inputs to multiplexers 911, 912, and 913 (multiplexing circuit). Hayashi et al. also teaches multiplexers 911, 912, and 913, (first level of glitchless multiplexers) that feed into multiplexer 93 (second level glitchless multiplexer) to serialize data transmitted over transmission line 200. Hayashi et al. fails to teach that data is transferred on both a rising edge and a falling edge of a clock signal. However, Kosco teaches a dual edge D flip flop circuit in Figure 2 that clocks data on both the rising and the falling edge of a clock signal as described in column 3, lines 18-35. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the teachings of Hayashi et al. with the dual edge

triggered clocking method of Kosco. A motivation for doing so would be to double the data throughput as stated in lines 1 and 2 of the abstract of Kosco.

Regarding claim **2**, Hayashi et al. further teaches multiplexers 911 and 912 (first level of two glitchless multiplexers) that each have a first input, a second input, an output and a control in Figure 17. Hayashi et al. also teaches a multiplexer 93 (second level single glitchless multiplexer) that has two input points, an output point and a control point from control circuit 96 in Figure 17. Multiplexers 911 and 912 (first level of glitchless multiplexers) receive data from latch circuits 901 and 902 (memory) and the outputs of these two multiplexers are fed into the inputs of multiplexer 93 (single glitchless multiplexer).

3. Claims **3 and 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (U.S. 6,556,583) in view of Kosco (U.S. 5,793,236) and in further view of Xi et al. (U.S. 5,982,309).

Regarding claim **3**, Hayashi et al. in view of Kosco teaches the network switch as recited in claims **1 and 2**. Hayashi et al. in view of Kosco fails to teach two additional multiplexers, each having two input connections, an output connection, and a control connection, that receive data and input that data into first and second inputs of the first level of glitchless multiplexers. However, Xi et al. teaches a parallel-to-serial CMOS data converter that makes use of multiple levels of 2:1 multiplexers to serialize input data in Figure 6. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the multilevel multiplexing of Xi et al. with the double data rate parallel-to-serial conversion teachings of Hayashi et

al. in view of Kosco. A motivation for doing so would be to provide parallel-to-serial conversion suitable for use in high-speed data links as described in column 2, lines 23-31 of the Xi et al. reference.

Regarding claim **4**, Hayashi et al. teaches flip-flop circuits 94, 921, 922, and 923 (plurality of flip flop circuits) that each have an input port, an output port and a clock input connected to a clock signal that provide feedback output signals that control the flow of data to multiplexers 911, 912, and 913 (first level of glitchless multiplexers). Hayashi et al. fails to teach that these flip-flop circuits control the flow of data to additional multiplexers. However, However, Xi et al. teaches a parallel-to-serial CMOS data converter that makes use of multiple levels of 2:1 multiplexers in conjunction with multiple D flip-flops controlled by shift clocks (SHIFTCLK1 – SHIFTCLK3) to serialize input data in Figure 6. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine the multilevel multiplexing with a D flip-flop matrix as in Xi et al. with the double data rate parallel-to-serial conversion teachings of Hayashi et al. in view of Kosco. A motivation for doing so would be to provide parallel-to-serial conversion suitable for use in high-speed data links as described in column 2, lines 23-31 of the Xi et al. reference.

4. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (U.S. 6,556,583) in view of Kosco (U.S. 5,793,236), and in further view of Raghunathan et al. (U.S. 6,324,679).

Regarding claim **5**, Hayashi et al. teaches a method of sending data over transmission line 200 (high performance interface) by receiving data in parallel at latch

circuits 901, 902 and 903 in Figure 17. This parallel data is multiplexed in multiplexers 911, 912, 913, and 93 in Figure 17. Data output from latch circuit 901 (one portion) is input into multiplexer 911 (first, first level glitchless multiplexer) while data output from latch circuit 902 (another portion) is input into multiplexer 912 (second, first level glitchless multiplexer). These portions are multiplexed based on signals (multiplexer selection signals) received from control circuit 96, and the outputs of multiplexers 911 and 912 are input into multiplexer 93 (second level glitchless multiplexer). Hayashi et al. fails to teach the storing of portions of data in latch 901 (a first register) clocked on a positive edge of a clock signal and latch 902 (a second register) clocked on a negative edge of a clock signal. However Kosco teaches a dual edge D flip-flop in Figure 2 that includes an upper latch stack 4 (first register) responsive to a clock rising edge and a lower latch stack 6 (second register) responsive to a clock falling edge. These dual edge triggered latch stacks could be used in place of latches 901 and 902 of the Hayashi et al. reference.

Hayashi et al. in view of Kosco fails to teach multiplexing data by selecting alternating inputs to be multiplexed onto the output of a second level glitchless multiplexer based on a multiplexer selection signal input into the second level glitchless multiplexer. Hayashi et al. in view of Kosco also fails to teach that the first level of glitchless multiplexers produces a function hazard when more than one input to a first level glitchless multiplexer changes simultaneously. Hayashi et al. in view of Kosco also fails to teach that selecting alternating inputs is timed so that the second level glitchless multiplexer only selects input from one of the first level multiplexers that is not

producing the function hazard. However, Raghunathan et al. teaches in Figure 14a – Figure 14c how a 2:1 multiplexer is used to select a glitchy data input as infrequently as possible. In these figures, signal Y is glitch-free while the output of subtractors 14a1 and 14c1 has a lot of glitches. By forcing the select signal to a specific value, the glitchy data input is selected as infrequently as possible as described in column 16, lines 10-35. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to use the multiplexer input selection method of Raghunathan et al. with the double data rate parallel-to-serial conversion teachings of Hayashi et al. in view of Kosco. A motivation for doing so would be to reduce the propagation of glitches to the multiplexer output as stated in column 16, lines 33-35 of the Raghunathan et al. reference.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hasegawa (U.S. 6,188,339), Baker et al. (U.S. 6,178,186), Heimann (U.S. 5,357,146), Mendel et al. (U.S. 6,359,469), Percey (U.S. 6,400,735), Luedtke (U.S. 5,481,215), Varma et al. (U.S. 5,831,980), Sandner (U.S. 6,075,392), Bertolet et al. (U.S. 6,025,744), Rasmussen (U.S. 5,231,636), Filip (U.S. 6,081,572), and Shimada et al. (U.S. 5,726,990) are all references that contain material pertinent to this application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Moore, Jr. whose telephone number is (703)

305-8703. The examiner can normally be reached on Monday-Friday (8:30am - 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached at (703) 308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael J. Moore, Jr.
Examiner
Art Unit 2666

mjm MM